

***AMD Embedded  
PCIe® ADD-IN BOARD  
E6760/E6460 Datasheet  
AEGX-A5T7-90FMT1\AEGX-A5T7-90FST1***

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## 1. Feature

| Model Name  | AEGX-A5T7-90FMT1                                      | AEGX-A5T7-90FST1 |
|---|---|------------------|
| Graphics Processing Unit                            |   |                  |
| GPU   | AMD Radeon E6760                                      |                  |
| Process Technology                                  | 40 nm   |                  |
| Graphics Engine Operating Frequency (max)           | 600 MHz   |                  |
| Form Factor   | ATX (145 x 110 mm)                                    |                  |
| GPU Interface                                       | PCI Express® 2.1 (X16)                                |                  |
| Shader Processing Units                             | 6 SIMD engines x 80 processing elements = 480 shaders |                  |
| Floating Point Performance (single precision, peak) | 576 GFLOPs  |                  |
| DirectX® capability                                 | DirectX® 11   |                  |
| Shader Model  | Shader Model 5.0                                      |                  |
| OpenGL  | OpenGL 4.1  |                  |
| OpenCL™ compliant                                   | AMD APP8, OpenCL™ 1.19, DirectCompute 11              |                  |
| Unified Video Decoder (UVD)                         | UVD3 for H.264, VC-1, MPEG-2, MPEG-4 part 2 decode    |                  |
| Memory  |   |                  |
| Operating Frequency (max)                           | 800 MHz / 3.2 Gbps                                    |                  |
| Configuration, type                                 | 128-bit wide, 1 GB, GDDR5, 51.2 GB/s                  |                  |
| Display Interfaces                                  |   |                  |
| Single / Dual-link DVI                              | Dual-Link DVI-I x 1 , Single Link DVI-I x1            |                  |
| Thermal Solution                                    |   |                  |
| Fansink / Fanless                                   | Fansink   | Fanless          |

## 2. Functional Overview

### 2.1. Memory Interface

AMD Radeon E6760 has four DRAM sequencers, E6460 has two DRAM sequencers. Each DRAM channel is 32-bit wide. Four/two 32 Mb × 32 GDDR5 memory chips are embedded on the ASIC for a total of 1G/512 MB Memory.

### 2.2. Acceleration Features

- Fully DirectX® 11 compliant, including full-speed 32-bit floating point per component operation:
- Shader Model 5.0 geometry and pixel support in a unified shader architecture.
- Support for OpenGL 4.1.
- Support for OpenCL™ 1.1
- Anti-aliasing filtering:
  - 2x/4x/8x/16x modes.
  - Multi-sample algorithm with gamma correction, programmable sample patterns, and centroid sampling.
  - Temporal anti-aliasing.
  - Adaptive anti-aliasing mode.
  - Lossless color compression (up to 8:1).
- Anisotropic filtering:
  - 2x/4x/8x/16x modes.
  - Up to 128-tap texture filtering.
  - Anisotropic biasing to allow trading quality for performance.
  - Improved quality mode due to improved sub pixel precision and higher precision LOD computations.
  - Advanced texture compression (3Dc+™).
  - High quality 4:1 compression for normal and luminance maps.
  - Works with any single- or two-channel data format
- Up to 16k × 16k textures, including 128-bit/pixel texture are supported.
- Fully associative texture, color, and z-cache design.
- Hierarchical z- and stencil-buffers with early z-test.

- Fast z-buffer clear.
- Fast color-buffer clear.

## 2.3. Avivo™ Display System

The AMD Avivo™ display system supports VGA, VESA super VGA, and accelerator mode graphics display on six independent display controllers. The full features of the AMD Avivo display system are outlined in the following sections.

## 2.4. DVI/HDMI Features

- Advanced DVI capability supporting 10-bit HDR (high dynamic range) output.
- Supports industry-standard CEA-861B video modes including 480p, 720p, 1080i, and 1080p. For a full list of currently supported modes, contact your local AMD support person.
- Maximum pixel rates for 24-bpp outputs are:
  - DVI—162 MP/s (megapixels per second) per link for 30-bpp dual-link; double for 24-bpp dual-link.
  - HDMI—148.5 MP/s.
- Fully compliant with the DVI electrical specification.

## 2.5. DisplayPort Features

### 2.5.1 DisplaPort 1.1a Features

- Supports all the mandatory features of the DisplayPort Version 1.1a Specification and the following optional features on all links:
  - 30-bit support.
  - YCbCr 444 up to 30-bpp and 422 up to 20-bpp support.
  - HDCP support.
  - DisplayPort extension for test-automation features, including test-pattern generation.
  - DisplayPort audio.
- Each DisplayPort link can support three options for the number of lanes and two options for link-data rate as follows:
  - Four, two, or one lane(s).

- 2.7- or 1.62-GHz link-data rate per lane.
- Supports all video modes supported by the display controller that do not over subscribe the link bandwidth.
  - Examples of supported pixel-rate/resolution support for four lanes at 2.7- GHz link rate:
    - Link bandwidth allows pixel clocks of up to 359 MP/s for 24 bpp or 287 MP/s for 30 bpp.
    - 2560 × 1600 @ 60Hz, 24 bpp is supported.
  - Examples of supported pixel-rate/resolution support for two lanes at 2.7- GHz link rate:
    - Link bandwidth allows pixel clocks of up to 179 MP/s for 24 bpp or 143 MP/s for 30 bpp.
    - 1920 × 1200 @ 60Hz, 24 bpp is supported.
  - The following table shows the maximum pixel rates for four, two, or one lane(s) at 2.7-GHz link rate.

## 2.5.2 DisplayPort 1.2 Features

- Each DisplayPort 1.2 link can transport up to six video streams; one from each display engine.
- Each DisplayPort link can support three options for the number of lanes and three options for link-data rate as follows:
  - Four, two, or one lane(s).
  - 5.4-, 2.7-, or 1.62-GHz link-data rate per lane.
- Supports all video modes supported by the display controller that do not oversubscribe the link bandwidth.
  - Examples of supported pixel-rate/resolution support for four lanes at 5.4- GHz link rate:
    - Link bandwidth allows pixel clocks of up to 718 MP/s for 24 bpp or 574 MP/s for 30 bpp.
    - 2560 × 2048 @ 60Hz, 30 bpp is supported.
  - Examples of supported pixel-rate/resolution support for two lanes at 5.4- GHz link rate:
    - Link bandwidth allows pixel clocks of up to 359 MP/s for 24 bpp or 287 MP/s for 30 bpp.
    - 2560 × 1600 @ 60Hz, 30 bpp is supported.

## 2.6. CRT DAC

- One integrated triple 10-bit DAC with built-in reference circuit.
- Single RGB-CRT output.
- Maximum pixel frequency of 400 MHz.
- Individual power-down feature for each of the three guns.

## 2.7. Bus Support Features

- Fully compliant with the PCI Express® Base Specification Revision 2.1.
- Supports ×1, ×2, ×4, ×8, and ×16 lane widths.
- Supports 2.5 GT/s and 5.0 GT/s link-data rates.

## 3. PIN Assignment and Description

| Pin                   | Side B Connector |   | Side A Connector |                                       |
|-----------------------|------------------|---|------------------|---------------------------------------|
| #                     | Name             | Description                                 | Name             | Description                           |
| 1                     | +12v             | +12 volt power                              | PRSNT#1          | Hot plug presence detect              |
| 2                     | +12v             | +12 volt power                              | +12v             | +12 volt power                        |
| 3                     | RSVD             | Reserved                                    | +12v             | +12 volt power                        |
| 4                     | GND              | Ground                                      | GND              | Ground                                |
| 5                     | SMCLK            | SMBus clock                                 | JTAG2            | TCK                                   |
| 6                     | SMDAT            | SMBus data                                  | JTAG3            | TDI                                   |
| 7                     | GND              | Ground                                      | JTAG4            | TDO                                   |
| 8                     | +3.3v            | +3.3 volt power                             | JTAG5            | TMS                                   |
| 9                     | JTAG1            | +TRST#                                      | +3.3v            | +3.3 volt power                       |
| 10                    | 3.3Vaux          | 3.3v volt power                             | +3.3v            | +3.3 volt power                       |
| 11                    | WAKE#            | Link Reactivation                           | PWRGD            | Power Good                            |
| <b>Mechanical Key</b> |                  |   |                  |                                       |
| 12                    | RSVD             | Reserved                                    | GND              | Ground                                |
| 13                    | GND              | Ground                                      | REFCLK+          | Reference Clock<br>Differential pair  |
| 14                    | HSOp(0)          | Transmitter Lane<br>0,<br>Differential pair | REFCLK-          |                                       |
| 15                    | HSOn(0)          |   | GND              | Ground                                |
| 16                    | GND              | Ground                                      | HSIp(0)          | Receiver Lane 0,<br>Differential pair |
| 17                    | PRSNT#2          | Hotplug detect                              | HSIn(0)          |                                       |
| 18                    | GND              | Ground                                      | GND              | Ground                                |
| 19                    | HSOp(1)          | Transmitter Lane<br>1,                      | RSVD             | Reserved                              |
| 20                    | HSOn(1)          |   | GND              | Ground                                |



| Pin | Side B Connector |  | Side A Connector |                                       |
|-----|------------------|--|------------------|---------------------------------------|
| #   | Name             | Description                              | Name             | Description                           |
|     |                  | Differential pair                        |                  |                                       |
| 21  | GND              | Ground                                   | HSIp(1)          | Receiver Lane 1,<br>Differential pair |
| 22  | GND              | Ground                                   | HSIn(1)          |                                       |
| 23  | HSOp(2)          | Transmitter Lane 2,<br>Differential pair | GND              | Ground                                |
| 24  | HSOn(2)          |  | GND              | Ground                                |
| 25  | GND              | Ground                                   | HSIp(2)          | Receiver Lane 2,<br>Differential pair |
| 26  | GND              | Ground                                   | HSIn(2)          |                                       |
| 27  | HSOp(3)          | Transmitter Lane 3,<br>Differential pair | GND              | Ground                                |
| 28  | HSOn(3)          |  | GND              | Ground                                |
| 29  | GND              | Ground                                   | HSIp(3)          | Receiver Lane 3,<br>Differential pair |
| 30  | RSVD             | Reserved                                 | HSIn(3)          |                                       |
| 31  | PRSNT#2          | Hot plug detect                          | GND              | Ground                                |
| 32  | GND              | Ground                                   | RSVD             | Reserved                              |
| 33  | HSOp(4)          | Transmitter Lane 4,<br>Differential pair | RSVD             | Reserved                              |
| 34  | HSOn(4)          |  | GND              | Ground                                |
| 35  | GND              | Ground                                   | HSIp(4)          | Receiver Lane 4,<br>Differential pair |
| 36  | GND              | Ground                                   | HSIn(4)          |                                       |
| 37  | HSOp(5)          | Transmitter Lane 5,<br>Differential pair | GND              | Ground                                |
| 38  | HSOn(5)          |  | GND              | Ground                                |
| 39  | GND              | Ground                                   | HSIp(5)          | Receiver Lane 5,<br>Differential pair |
| 40  | GND              | Ground                                   | HSIn(5)          |                                       |
| 41  | HSOp(6)          | Transmitter Lane 6,<br>Differential pair | GND              | Ground                                |
| 42  | HSOn(6)          |  | GND              | Ground                                |
| 43  | GND              | Ground                                   | HSIp(6)          | Receiver Lane 6,<br>Differential pair |
| 44  | GND              | Ground                                   | HSIn(6)          |                                       |
| 45  | HSOp(7)          | Transmitter Lane 7,                      | GND              | Ground                                |

| Pin | Side B Connector |                      | Side A Connector |  |
|-----|------------------|----------------------|------------------|--|
| #   | Name             | Description          | Name             | Description                            |
| 46  | HSOn(7)          | Differential pair    | GND              | Ground                                 |
| 47  | GND              | Ground               | HSIp(7)          | Receiver Lane 7,<br>Differential pair  |
| 48  | PRSNT#2          | Hot plug detect      | HSIn(7)          |  |
| 49  | GND              | Ground               | GND              | Ground                                 |
| 50  | HSOp(8)          | Transmitter Lane 8,  | RSVD             | Reserved                               |
| 51  | HSOn(8)          | Differential pair    | GND              | Ground                                 |
| 52  | GND              | Ground               | HSIp(8)          | Receiver Lane 8,<br>Differential pair  |
| 53  | GND              | Ground               | HSIn(8)          |  |
| 54  | HSOp(9)          | Transmitter Lane 9,  | GND              | Ground                                 |
| 55  | HSOn(9)          | Differential pair    | GND              | Ground                                 |
| 56  | GND              | Ground               | HSIp(9)          | Receiver Lane 9,<br>Differential pair  |
| 57  | GND              | Ground               | HSIn(9)          |  |
| 58  | HSOp(10)         | Transmitter Lane 10, | GND              | Ground                                 |
| 59  | HSOn(10)         | Differential pair    | GND              | Ground                                 |
| 60  | GND              | Ground               | HSIp(10)         | Receiver Lane 10,<br>Differential pair |
| 61  | GND              | Ground               | HSIn(10)         |  |
| 62  | HSOp(11)         | Transmitter Lane 11, | GND              | Ground                                 |
| 63  | HSOn(11)         | Differential pair    | GND              | Ground                                 |
| 64  | GND              | Ground               | HSIp(11)         | Receiver Lane 11,<br>Differential pair |
| 65  | GND              | Ground               | HSIn(11)         |  |
| 66  | HSOp(12)         | Transmitter Lane 12, | GND              | Ground                                 |
| 67  | HSOn(12)         | Differential pair    | GND              | Ground                                 |
| 68  | GND              | Ground               | HSIp(12)         | Receiver Lane 12,<br>Differential pair |
| 69  | GND              | Ground               | HSIn(12)         |  |
| 70  | HSOp(13)         | Transmitter Lane 13, | GND              | Ground                                 |
| 71  | HSOn(13)         | Differential pair    | GND              | Ground                                 |

| Pin | Side B Connector |   | Side A Connector |  |
|-----|------------------|---|------------------|--|
| #   | Name             | Description                               | Name             | Description                            |
| 72  | GND              | Ground                                    | HSIp(13)         | Receiver Lane 13,<br>Differential pair |
| 73  | GND              | Ground                                    | HSIn(13)         |  |
| 74  | HSOp(14)         | Transmitter Lane 14,<br>Differential pair | GND              | Ground                                 |
| 75  | HSOn(14)         |   | GND              | Ground                                 |
| 76  | GND              | Ground                                    | HSIp(14)         | Receiver Lane 14,<br>Differential pair |
| 77  | GND              | Ground                                    | HSIn(14)         |  |
| 78  | HSOp(15)         | Transmitter Lane 15,<br>Differential pair | GND              | Ground                                 |
| 79  | HSOn(15)         |   | GND              | Ground                                 |
| 80  | GND              | Ground                                    | HSIp(15)         | Receiver Lane 15,<br>Differential pair |
| 81  | PRSNT#2          | Hot plug present<br>detect                | HSIn(15)         |  |
| 82  | RSVD#2           | Hot Plug Detect                           | GND              | Ground                                 |

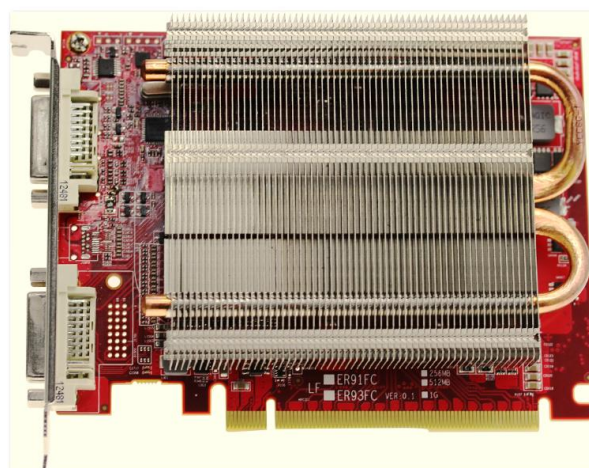
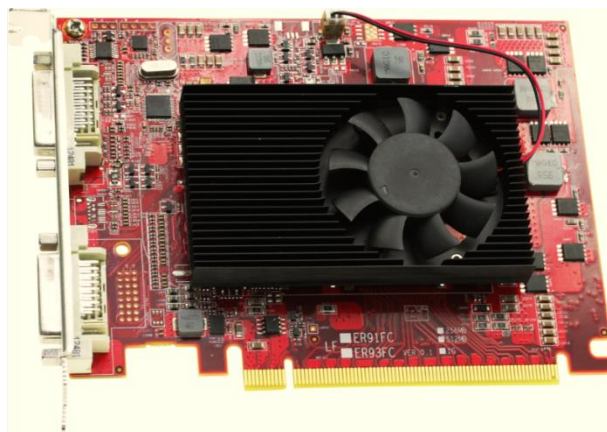
## 4. Power Consumption

| Application          | Total ASIC Power + DRAM Power (W) |
|----------------------|-----------------------------------|
| Static Windows - 65c | <b>7.73</b>                       |

| Application         | Total ASIC Power + DRAM Power (W) |
|---------------------|-----------------------------------|
| 3D Mark Vantage FT6 | <b>28.02</b>                      |

## 5. Output configuration and Board Dimension

### 5.1. Output Configuration

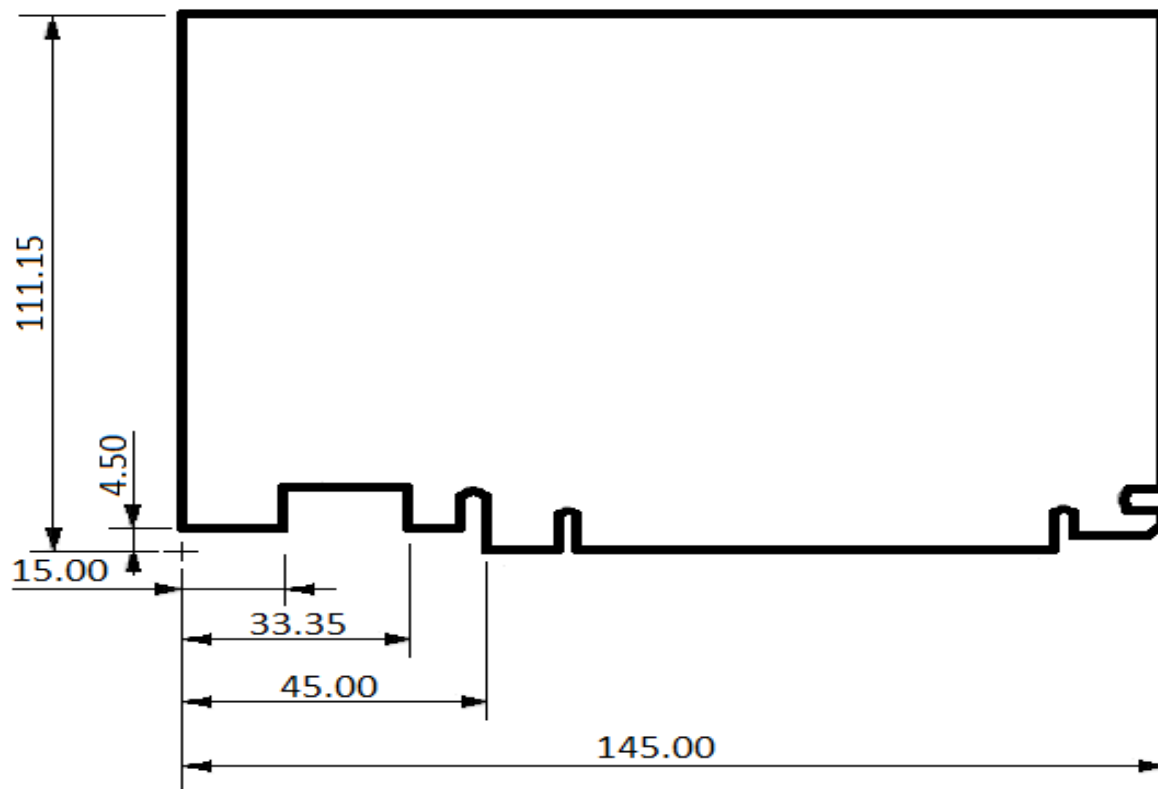


Single link DVI-I

Dual link DVI-I

### 5.2 Board Dimension

(Unit : mm)

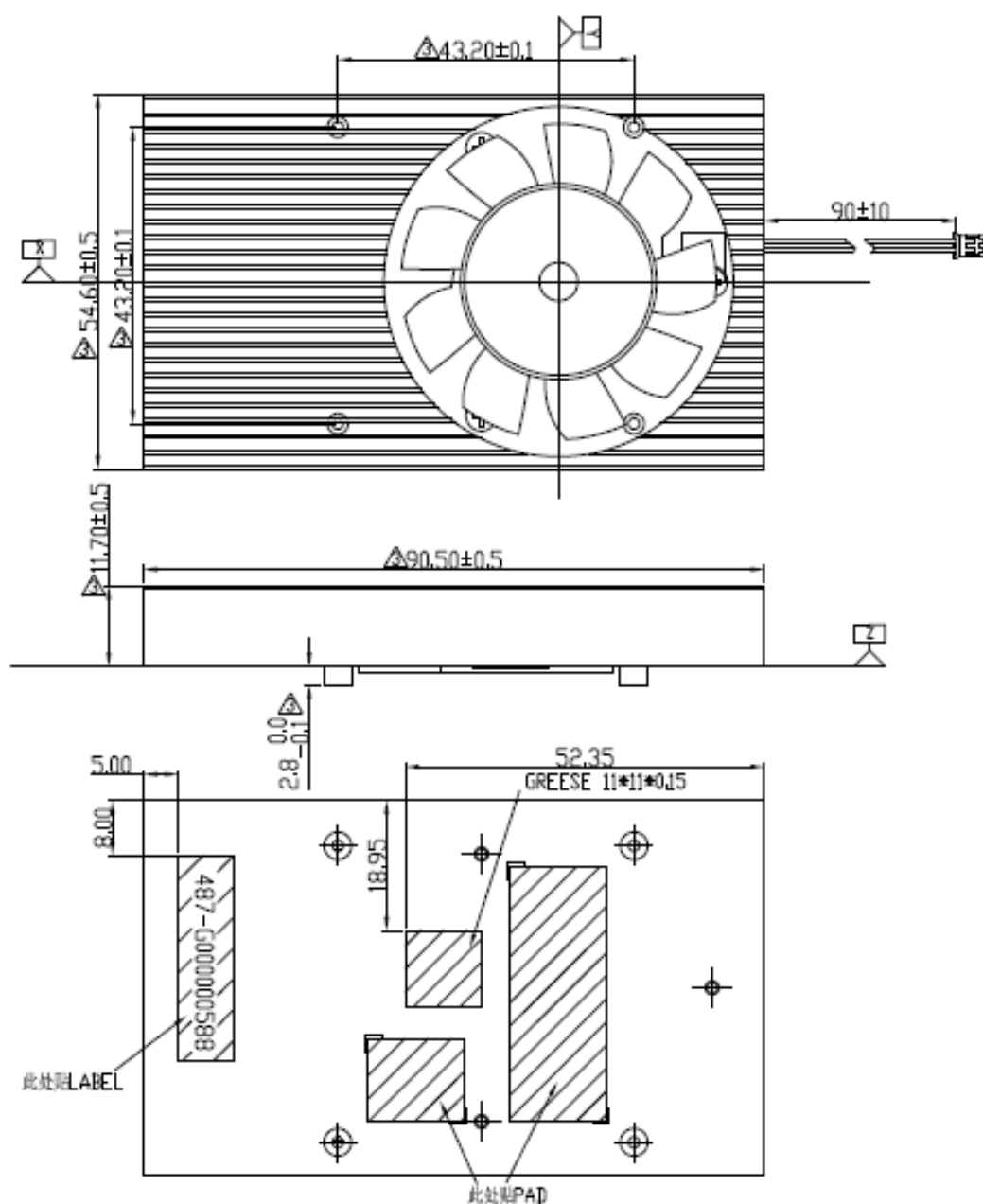


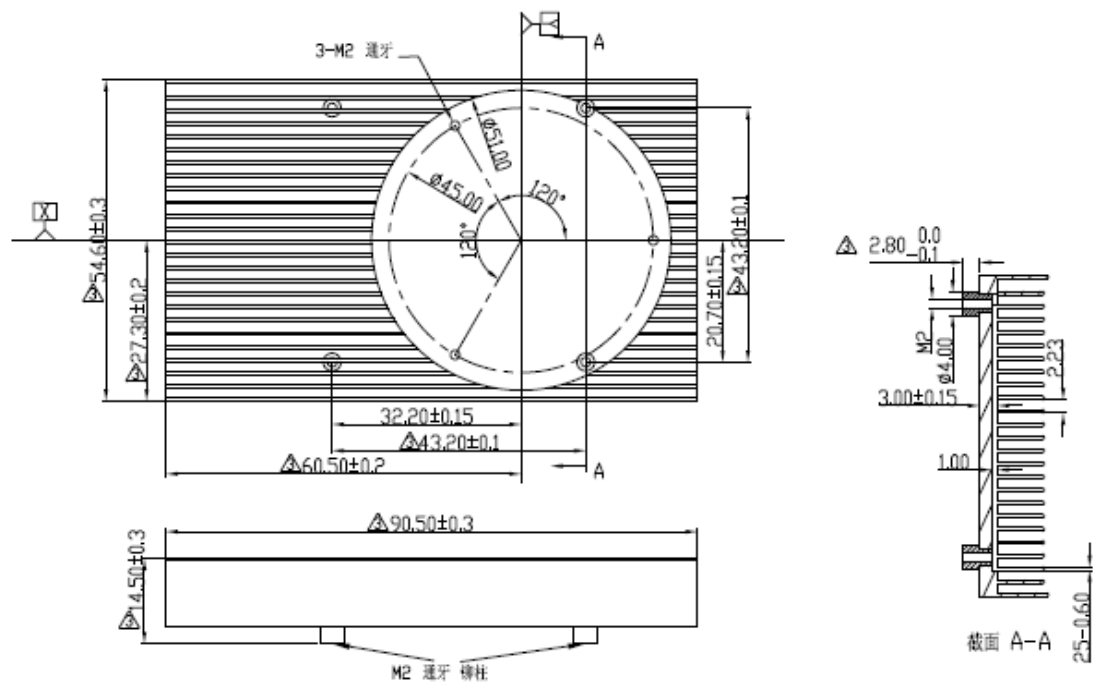
Tolerances :  $\pm 0.13$  mm

## 6. Thermal Mechanism

### 6.1. Fan-sink Thermal Module

(Unit : mm)



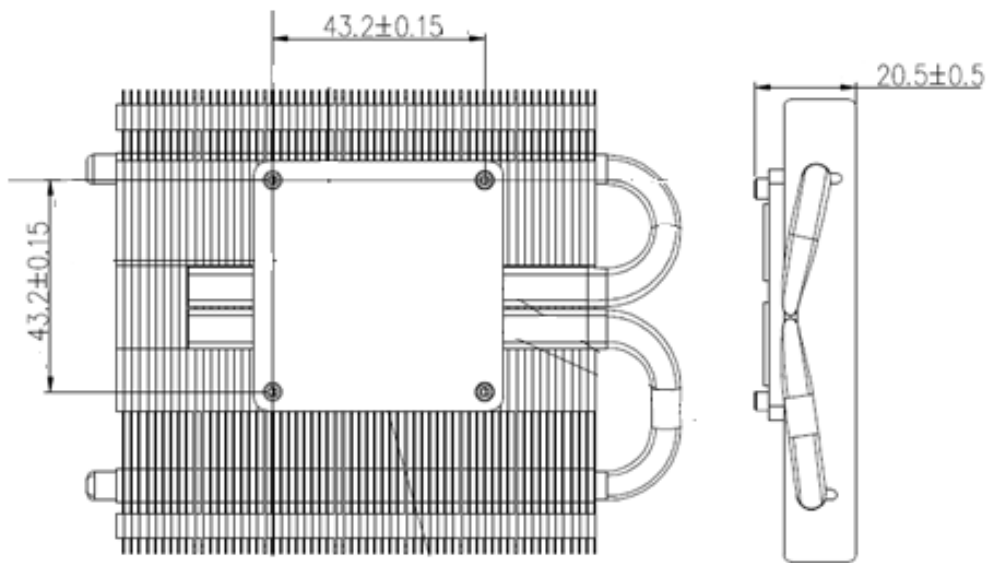


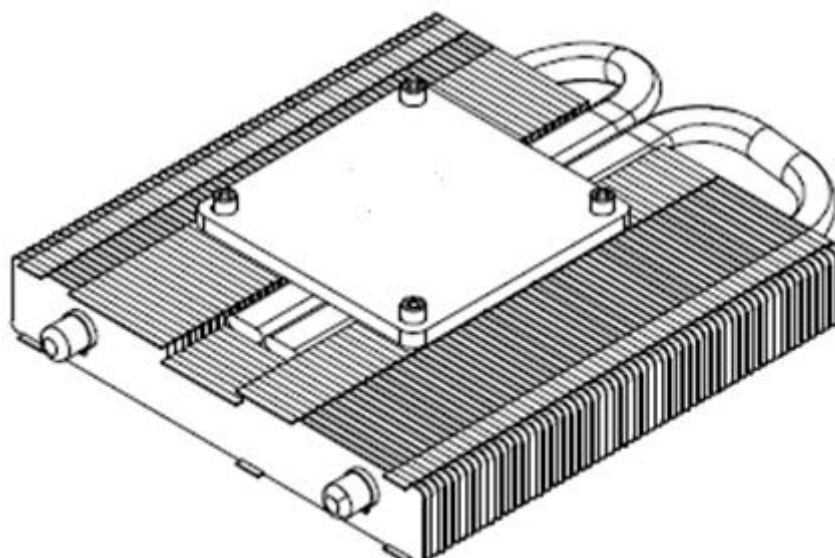
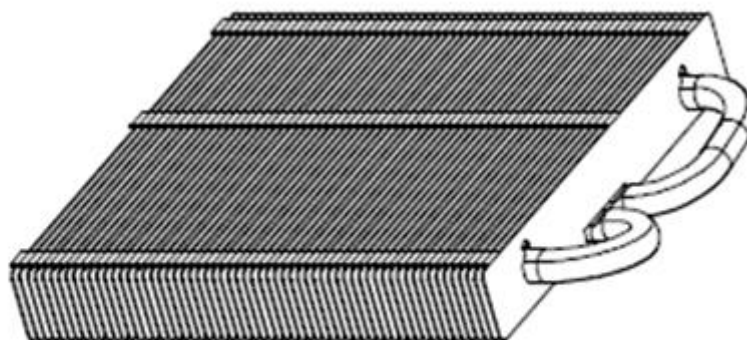
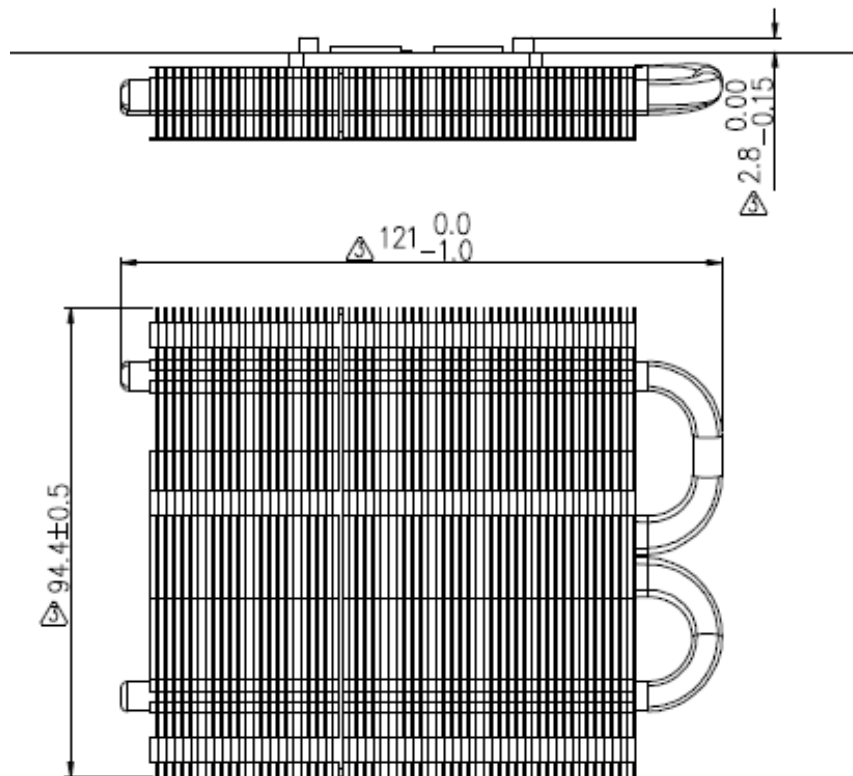
| Tolerances |          |
|------------|----------|
| 0-10       | +/- 0.1  |
| 10-50      | +/- 0.15 |
| 50-100     | +/- 0.2  |
| 100~       | +/- 0.25 |



## 6.2. Passive Thermal Module

(Unit : mm)





| Tolerances |          |
|------------|----------|
| 0-10       | +/- 0.1  |
| 10-50      | +/- 0.15 |
| 50-100     | +/- 0.2  |
| 100~       | +/- 0.25 |

## 7. Order Information

| Model            | GPU   | Form Factor        | DVI | Bracket     | Thermal Solution |
|------------------|-------|--------------------|-----|-------------|------------------|
| AEGX-A5T7-90FMT1 | E6760 | ATX (145 x 110 mm) | 2   | Full Height | Fansink          |
| AEGX-A5T7-90FST1 | E6760 | ATX (145 x 110 mm) | 2   | Full Height | Fanless          |

## 8. Change Log Update History

| Rev. | Data       | History               |
|------|------------|-----------------------|
| 0.1  | 2015/09/16 | 1 <sup>st</sup> Draft |